WHAT IS CLAIMED IS:

1. A controller for generating a control signal for driving an electrical load, comprising:

a signal generator for repeatedly generating and outputting pulse-width-modulated signals based on drive data representing signal hold times at respective first and second levels per signal cycle;

a calculator for calculating said drive data at a predetermined calculation cycle and storing said drive data in a data storage device;

a clock for repeatedly clocking a half-cycle time of said pulse-width-modulated signal asynchronously from said calculation cycle of said calculator;

period establishing means for, at first and second determination periods, establishing respective clock periods which are said half-cycle times clocked by said clock in an alternating manner;

drive-data acquiring means for acquiring drive data from said data storage device at each clocking start of said half-cycle time by said clock; and

signal level determining means for determining, when a clock period of said clock has been established by said period-determining means at said first determining period and based on drive data acquired by said drive-data acquiring means, whether said clock time according to said clock has reached a second time which is half of a time at which said signal per pulse-

width-modulated signal cycle is to be held at a second level, and when determined to have reached said second time, to establish a signal level of said pulse-width-modulated signal at a first level, and to determine, when a clock period of said clock has been established by said period-determining means at said second determining period and based on drive data acquired by said drive-data acquiring means, whether said clock time according to said clock has reached a first time which is half of a time at which said signal per pulse-width-modulated signal cycle is to be held at a first level, and when determined to have reached said first time, to establish a signal level of said pulse-width-modulated signal at a second level;

said signal generator for outputting a pulse-width-modulated signal at a signal level established by said signal-level determining means.

2. A controller as recited in claim 1, wherein said drive-data acquiring means continuously acquires and updates said drive data at said data storage device in an interval from when said clock starts clocking said half-cycle time until said level-determining means determines that said drive data has reached one of said first and second times.

3. A controller as recited in claim 1, further comprising:

a monitor for monitoring whether drive data stored at said data storage device is updated by operation of said

calculator in an interval from when said clock starts clocking said half-cycle time until said clock starts clocking a subsequent half-cycle time, and when updating of said drive data is detected, to cause said drive-data acquiring means to operate asynchronously from said clock to cause drive data which said signal-level determining means utilizes in determining clock time to be updated with newest drive data at data storage device; and

means for prohibiting level inversion to stop determining operation of said signal-level determining means and prohibit inversion of a signal level of said pulse-width-modulated signal in an interval from when said clock starts clocking said half-cycle time until when said signal-level determining means determines that clock time according to said clock has reached one of said first time and second times, thereafter said clock clocking a subsequent half-cycle time.

4. A controller as recited in claim 1, wherein:

said signal generator is utilized in a conductivity controller for an electrical load to cause said drive data corresponding to pulse-width-modulated signals to respective conductors to allow current to flow individually to two electrical loads to be individually calculated by said calculator and to be stored in first and second data storage devices;

two devices other than said clock and said period-determining means are caused to respectively correspond to said first and second data storage devices; and

one of two signal-level determining means determines when a clock period of said clock has been established by said period-determining means at said second determining period and based on drive data acquired by said drive-data acquiring means, whether clock time according to said clock has reached a second time which is half of a time at which said signal per pulse-width-modulated signal cycle is to be held at a second level, and when determined to have reached said second time, to establish a signal level of said pulse-width-modulated signal at a first level; and

when a clock period of said clock has been established by said period-determining means at said first determining period and based on drive data acquired by said drive-data acquiring means, to determine whether clock time according to said clock has reached a first time which is half of a time at which said signal per pulse-width-modulated signal cycle is to be held at a first level, and when determined to have reached said first time, to establish a signal level of said pulse-width-modulated signal at a second level;

said signal generator for outputting respective pulse-width-modulated signals at signal levels individually established by said two signal-level determining means.

5. A controller as recited in of claim 1, wherein:

said clock comprises one of a down counter and an up counter for changing a count value by a predetermined number at every fixed time interval, and for causing a count value to experience two iterations with one cycle time of said pulse-width-modulated signal.

6. A controller for generating a control signal for driving a target load, comprising:

a microcomputer for cyclically generating and outputting pulse-width-modulated drive signals based on acquired drive data, for establishing clock periods which are alternating half-cycle clocked times, and for acquiring said drive data at each start of said half-cycle clocked times;

a switch connected between said microcomputer and said target load for switchably connecting said target load to a power source based on said drive data to selectively drive said target load; and

a feedback loop between said target load and said microcomputer for providing actual target load drive data to said microcomputer;

said microcomputer adjusting said pulse-width-modulated drive signals at a rate of not more than two times per cycle based on said actual target load drive data to converge said actual target load drive data to a calculated target load drive value.

7. A controller as recited in claim 6, wherein said microcomputer adjusts said pulse-width-modulated drive signals at rising and falling edges of said signal.

8. A controller as recited in claim 6, wherein said microcomputer includes a pulse-width-modulated output portion for generating said pulse-width-modulated drive signals based on said acquired drive data.

9. A controller as recited in claim 8, wherein said pulse-width-modulated output portion includes an up-down counter for each target load to be driven to determine a half-cycle time for each said target load.

10. A controller as recited in claim 8, wherein said pulse-width-modulated output portion includes a down counter for each target load to be driven to determine a half-cycle time for each said target load.

11. A controller as recited in claim 8, wherein said pulse-width-modulated output portion includes an up counter for repeatedly clocking a half-cycle time of said pulse-width-modulated signal.

12. A controller as recited in claim 8, wherein said drive data is updated at said pulse-width-modulated portion upon initiation of each of said half-cycle clocked times.

13. A controller as recited in claim 8, wherein said drive data is continuously updated at said pulse-width-modulated portion.

14. A controller as recited in claim 8, wherein said microcomputer generates update flags to indicate an update status of said drive data for each target drive load, said pulse-width-modulated portion re-setting each of said update flags when corresponding drive data has been used to generate said pulse-width-modulated signals.

15. A controller as recited in claim 8, wherein said pulse-width-modulated output portion includes a down counter for each pair of target loads to be driven to determine a half-cycle time for each pair of said target loads, said counter providing a normal count signal to a first of said pair of target loads, and an inverted count signal to a second of said pair of target loads.

16. A method for generating a control signal for driving a target load, comprising:

cyclically generating and outputting pulse-width-modulated drive signals based on acquired drive data, for establishing clock periods which are alternating half-cycle clocked times, and for acquiring said drive data at each start of said half-cycle clocked times;

switchably connecting said target load to a power source based on said drive data to selectively drive said target load;

providing actual target load drive data to said microcomputer; and

adjusting said pulse-width-modulated drive signals at a rate of not more than two times per cycle based on said actual target load drive data to converge said actual target load drive data to a calculated target load drive value.

17. The method of claim 16, further comprising the step of adjusting said pulse-width-modulated drive signals at rising and falling edges of said signal.

18. The method of claim 16, further comprising updating said drive data upon initiation of each of said half-cycle clocked times.

19. The method of claim 16, further comprising continuously updating said drive data.

20. The method of claim 16, further comprising the step of generating update flags to indicate an update status of said drive data for each target drive load; and

re-setting each of said update flags when corresponding drive data has been used to generate said pulse-width-modulated signals.

21. An apparatus for conditioning analog signals for control use, comprising:

an analog-to-digital converter for converting input signals to digital values at a conversion cycle shorter than an input cycle of said input signals;

a data storage device for sequentially storing said digital values obtained from said analog-to-digital converter; and

a processor for calculating a mean value to fetch said digital values at a cycle time m (where m is an integer) of said input signals from said data storage device, and for computing an arithmetic mean of said fetched digital values, for target control purposes.

22. A control apparatus, comprising:

a detector for detecting a predetermined operating state of a control target, and for generating a detection signal changing at a fixed detection signal cycle in correspondence with said operating state;

an analog-to-digital converter for fetching a detection signal from said detector and converting said detection signal to a digital value at a predetermined analog-to-digital conversion cycle; and

a controller for controlling said control target based on a digital value acquired from said analog-to-digital converter;

a storage device for storing said digital value converted by said analog-to-digital converter;

said analog-to-digital converter for converting a detection signal from said detector to a digital value at an analog-to-digital conversion cycle shorter than said detection signal cycle, and for sequentially storing converted digital values in said storage device; and

said controller including a calculator for calculating a mean value to fetch said stored digital values at a cycle time m (where m is an integer) of said input signal from said storage device, for computing an arithmetic mean of said fetched digital values, and for utilizing a computed digital result of said calculator to control said control target.

23. A control apparatus as recited in claim 22, wherein:

said detector detects a current flowing to an electrical load and changing at a fixed current cycle;

said analog-to-digital converter converts said detection signal from said detector to said digital value at an analog-to-digital conversion cycle shorter than said fixed current cycle;

said calculator calculates a current mean value of said current flowing to said electrical load by fetching said stored digital values from said storage device at said cycle time m of said current and computing an arithmetic mean of said fetched digital values; and

said controller controls a predetermined operating state of a control target including said electrical load based on said mean current value of said electrical load computed by said calculator.

24. A current-control apparatus, comprising:

a detector for detecting an electrical current flowing to an electrical load, said current being controlled by a pulse-width-modulated signal generated at a fixed control signal cycle;

an analog-to-digital converter for converting a detection signal from said detector to a digital value at a predetermined analog-to-digital conversion cycle shorter than said fixed control signal cycle; and

a controller for controlling a duty of said pulse-width-modulated signal so that a detected current value converted to a digital value by said analog-to-digital converter becomes a target current value;

a data storage device for storing said detected current value converted to a digital value by said analog-to-digital converter;

said analog-to-digital converter further for sequentially storing detection signals at said data storage device; and

said controller including a calculator for calculating a mean current value within cycle time m (where m is an integer) by fetching and computing an arithmetic mean of sequentially-

stored detected current values, and for controlling a duty of said pulse-width-modulated signal based on a mean current value, calculated by said calculator, and said target current value.

25. A current-control apparatus as recited in claim 24, wherein said calculator fetches 2^n detected current values as detected current values for cycle time m of said pulse-width-modulated signal, calculates a sum of said detected current values, and calculates said mean current value from said sum.

26. A current-control apparatus as recited in claim 24, wherein said calculator is provided with means for determining an abnormality to determine whether an abnormal current value exists in detected current values of cycle time m fetched from said data storage device, and when an abnormal current value is determined to exist, does not utilize said abnormal current value in calculating said mean current value.

27. A current-control apparatus as recited in claim 26, wherein when an abnormal current value is determined to exist, said calculator estimates a normal current value with an analog-to-digital conversion timing of an abnormal current value from detected current values which have undergone analog-to-digital conversion before and after said abnormal current value, and substitutes said estimated current value for said abnormal current value in calculating said mean current value.

28. A current-control apparatus as recited in claim 24, further comprising a filter for eliminating high-frequency noise provided in a signal input path from said detector to said analog-to-digital converter.

29. A current-control apparatus as recited in claim 24, wherein said current-value storage device stores only detected current values of cycle time m of said pulse-width-modulated signal received for said calculator to calculate said mean current value; and

said analog-to-digital converter sequentially updates, at said analog-to-digital conversion cycle, said sequentially-stored detected current values at said data storage device, by sequentially saving a newly detected digitally-converted current value at said data storage device.

30. A current-control apparatus as recited in claim 24, wherein said calculator operates at a predetermined operating cycle and calculates said mean current value together with a duty of said pulse-width-modulated signal based on said mean current value and said target current value; and

a signal generator for repeatedly generating a pulse-width-modulated signal in correspondence with said duty calculated by said calculator.

31. A current-control apparatus as recited in claim 30, wherein said analog-to-digital conversion cycle is not more

than a processing cycle whereat said calculator calculates said duty.

32. A current-control apparatus as recited in claim 30, wherein said calculator operates asynchronously from said analog-to-digital converter, and calculates said mean current value using respective detected current values stored at said data storage device.

33. A current-control apparatus as recited in claim 30, wherein said pulse-width-modulated signal generator and said analog-to-digital converter synchronously operate based on a clock signal from a common clock source.

34. A current-control apparatus, comprising:

a calculator for calculating a duty of a pulse-width-modulated signal to enable a predetermined current to flow to an inductive load at each iteration of a predetermined processing cycle; and

a generator for repeatedly generating a pulse-width-modulated signal in correspondence with a duty calculated by said calculator, and for outputting said pulse-width-modulated signal to a means for energizing said inductive load;

said calculator calculating, from said calculated duty, a level holding time at which said pulse-width-modulated signal is to be held at a first level and a second level each cycle of said pulse-width-modulated signal, and is provided with

a data storage device to save said level holding time as drive data;

said pulse-width-modulated signal generating circuit including a clock for repeatedly clocking a time of one-half of one cycle of said pulse-width-modulated signal asynchronously from a processing cycle of said calculator;

means for calculating an inversion time to acquire said drive data from said data storage device synchronously with said clocking operation of said clock, and to respectively calculate one-half of a time at which said signal per cycle of said pulse-width-modulated signal is to be held at a first level as a first time, and similarly a time at which said signal per cycle of said pulse-width-modulated signal is to be held at a second level as a second time;

means for determining clock time to determine, at each clock time whereat said clock clocks said one-half time of said pulse-width-modulated signal cycle time, whether said clock has reached a newest first time calculated by said inversion-time calculating means or whether said clock has reached a newest second time calculated by said inversion-time calculating means; and

means for establishing a signal level to establish said second level when said clock-time damage means determines that said clock has reached said first time, and to establish said first level when said clock-time damage means determines that said clock has reached said second time;

said pulse-width-modulated signal generating circuit outputting a pulse-width-modulated signal at a signal level established by said signal-level establishing means.

35. A current-control apparatus as recited in claim 34, further comprising:

a detector for detecting current flowing to said inductive load; and

an analog-to-digital converter for converting a detection signal from said detector to a digital value at a predetermined analog-to-digital conversion cycle;

wherein said calculator calculates, based on said detected current value, a target current value converted to a digital signal by said analog-to-digital converter, and a duty of said pulse-width-modulated signal required for controlling said detected current value at said target current value.

36. A current-control apparatus as recited in claim 34, wherein said pulse-width-modulated signal generator comprises:

a monitor for monitoring whether drive data stored at said data storage device is updated by operation on the calculator side from when said clock starts clocking said one-half time of said pulse-width-modulated signal one-cycle time until said clock starts clocking a subsequent one-half time; and

means for updating inversion time to cause, when updating of said drive data is detected by said monitor, said

inversion-time calculating means to operate asynchronously with respect to said clock and cause said first time and said second time which said clock-time determining means utilizes in determining clock time to be updated to a time corresponding to newest drive data at said data storage device.